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Influence of Highly Charged Ion Irradiation on the Electrical and Memory Properties of Black Phosphorus Field-Effect Transistors

Stephan Sleziona, Osamah Kharsah, Lucia Skopinski, Leon Daniel, Jennifer Schmeink, and Marika Schleberger**

Black phosphorus (bP) is one of the more recently discovered layered materials. Utilizing the hysteresis in the transfer characteristics of bP field-effect transistors (FETs), several approaches to realize non-volatile memory devices are successfully demonstrated. This hysteresis is commonly attributed to charge trapping and detrapping in impurities and defects whose nature and location in the device are however unclear. In this work, defects are deliberately introduced into bP FETs by irradiating the devices with highly charged Xe^{30+} at a kinetic energy of 180 and 20 keV to manipulate their electrical and memory properties. The results show for the ion with higher energy an increase of conductance and an increase of p-doping of up to 1.2 $\cdot$ 10^{12} cm^{-2} with increasing fluence, while the charge carrier mobility degrades for the higher ion fluences. Most notably, an increase in the hysteresis' width and of the memory window are observed due to the irradiation. By controlling the kinetic energy of the ions, it can be demonstrated, that the modifications of electronic properties arise from defects in bP and the underlying SiO_2 substrate. However, changes in hysteretic properties are attributed exclusively to irradiation-induced defects in the substrate, so ion irradiation can significantly improve the properties of bP based memory devices.

1. Introduction

Due to the ongoing miniaturization in modern-day electronics, ultrathin 2D materials are one of the most promising material classes for future developments in this field. Discovered as the first 2D material, graphene is not useful for opto-electronic applications because of the absence of the required bandgap.[1] Consequently, researchers have turned their attention to alternative 2D materials, notably transition-metal dichalcogenides (TMDCs), with MoS_2 emerging as a prominent representative within this category, garnering significant research focus over the last decade.[2,3] Typically, TMDCs display n-type semiconductor properties, and the main challenge for their practical utilization stems from the lack of adequate p-doping methods.[4] Hence, following its rediscovery as a layered material, there has been a recent surge of interest in thin layers of black phosphorus (bP) due to its rather unique properties, such as a high hole mobility of up to 1000 cm^2 V^{-1} s^{-1}, and its predominantly observed p-type behavior in devices like field-effect transistors (FETs).[5,6] In bP, the phosphorus atoms form a puckered honeycomb lattice through covalent bonds with three neighboring phosphorus atoms via sp^3 hybridized orbitals (see the schematic bP lattice in **Figure 1c**)). Due to the weak van der Waals bonding between individual layers, black phosphorus (bP) can be readily exfoliated to the monolayer level, with the bandgap shifting from 2.0 eV in the monolayer to ≈0.3 eV for thicknesses greater than 10 nm.[7,8]

There are many emerging novel applications of 2D materials and bP in particular. These applications include areas such as opto-electronics,[9,10] energy devices,[11,12] and especially non-volatile memory devices.[13–16] In comparison to TMDCs as a channel material for 2D memory devices, the high mobility of bP, while maintaining similar drain current modulation, makes it a promising candidate for such applications.[17–21] Note, that the degradation of bP in ambient conditions,[22] a well-known obstacle for its various applications, can be overcome by encapsulation techniques, utilizing e.g. hexagonal boron nitride (hBN),[23] aluminum oxide (Al_2O_3)[24] or polymethyl methacrylate (PMMA)[25] as a protective layer.

In a non-volatile memory device, a charge trapping layer is commonly employed, capable of storing charges through a gate pulse, thereby enabling the manipulation of current flowing through the channel material. But even a much simpler structure of a 2D material on a Si/SiO_2 substrate can already be

S. Sleziona, O. Kharsah, L. Skopinski, L. Daniel, J. Schmeink, M. Schleberger
Faculty of Physics and CENIDE
University of Duisburg-Essen
Lotharstraße 1, D-47057 Duisburg, Germany
E-mail: stephan.sleziona@uni-due.de; marika.schleberger@uni-due.de

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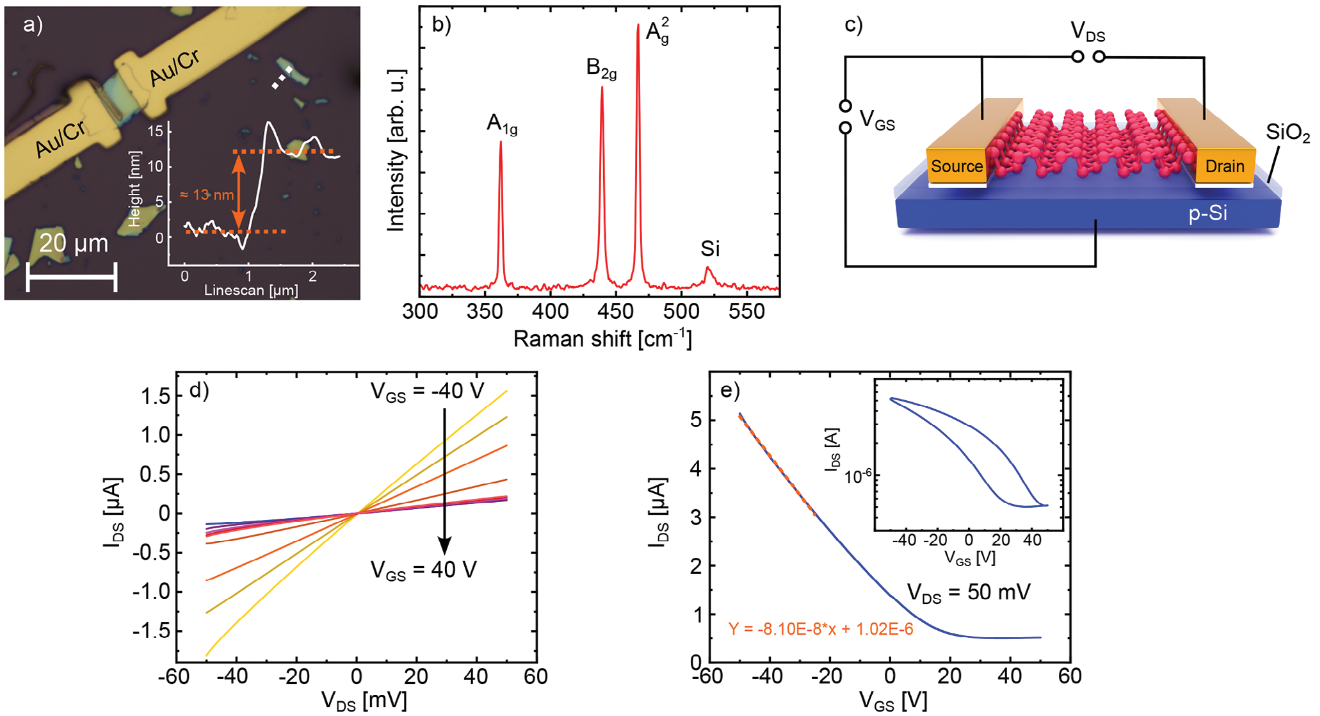

Figure 1. a) Optical microscopy image of one of the devices used in this work. The linescan in the lower right side of the image corresponds to an atomic force microscopy (AFM) measurement of the small flake marked by the white dotted line just above it. b) Raman spectrum of the bP channel displaying the typical bP Raman modes A_{1g}, B_{2g} and A_g^2. c) Outline of our device geometry and measurement setup. d) Typical output characteristics of one of our devices. e) Typical transfer characteristics of one of our devices. The inset shows the transfer characteristics on a logharithmic scale, measured for the gate-source voltage being swept from negative to positive values and back, demonstrating the hysteretic behavior.

utilized as a memory device by trapping and detrapping charges in defects.[25–27] The exact nature of defects responsible for causing the hysteresis in 2D FETs is still a subject of debate, whether they are located in the 2D material, at the 2D material/oxide interface or within the oxide itself.[28–33] These trapped charges commonly induce hysteresis in the transfer characteristics of these devices, when the gate voltage is swept from, e.g., negative to positive values and then back to negative values.

Artificial defects in these kind of devices can be created by particle irradiation such as electron or ion irradiation.[34–39] For monolayer MoS_2 it was already demonstrated, that ion irradiation can increase the hysteresis by seeding additional defects into the devices that contribute to charge trapping and detrapping, amplifying their memory properties.[40–42] As for bP, there is only one study carried out by Goyal et al.,[43] where the exposure to a keV electron beam led to improved standard electronic properties, including on-current and mobility, along with a decrease in hysteresis. These findings were tentatively attributed to the capture of electrons in traps near the SiO_2/bP interface and a decrease in bP surface roughness caused by the irradiation.

In our work, we aim to explore the potential and opportunities for altering the electrical and memory characteristics of ultrathin bP FETs in detail using ion irradiation. In particular, we aim to unambiguously determine the location of the respective defects and monitor their influence on the devices' properties. To this end, we utilize highly charged ions (HCIs) with a charge state of $q = 30+$ for irradiating our devices.

Charge state and kinetic energy can be chosen independently[44] and we can achieve very high kinetic energies, i.e. up to $E_{\text{kin}} = 260$ keV. This allows us to precisely control the depth at which the ion energy is deposited in our sample. This, in turn, means we can not only induce defects exclusively in the several tens of nm thick bP layer but also intentionally create defects in the underlying SiO_2. Specifically, $E_{\text{kin}} = 180$ keV results in defect formation occurring in both the bP channel and the underlying oxide, whereas with the lower kinetic energy of 20 keV, defect creation is confined to the bP layer alone. As a result, we are able to distinguish the effects of intrinsic defects in the bP from those of defects in the oxide on the properties of our devices. The irradiations took place in ultra-high vacuum conditions (see Experimenatal Section for details). The devices were stored in these conditions until they were transferred to our measurement setup, where electrical measurements were performed at in vacuum ($p \simeq 1 \cdot 10^{-2}$ mbar) to minimize the impact of adsorbates like water and oxygen molecules on the device properties and to prevent bP degradation. Furthermore, it is important to note, that for bP flakes with a thickness > 10 nm, the rate of degradation is quite low[45] and the electrical properties of corresponding bP FETs are stable against ambient degradation up to several days.[46] Indeed, we see no signs of degradation in the topography of our bP FETs after three consecutive irradiation-and-measurement steps, as confirmed by AFM (see Figure S1, Supporting Information).

We observe pronounced changes in the electrical properties of our devices, such as increased conductance and increased p-doping resulting from the irradiation at both kinetic energies. We utilize the inherent hysteresis in the transfer characteristics of our devices to realize a non-volatile memory device with two well-separated memory states and proceed to demonstrate that the irradiation with a kinetic energy of 180 keV increases the width of the hysteresis and the memory window of our devices. Interestingly, we find no such behavior for a device irradiated with ions with a kinetic energy of 20 keV, where the ions cannot transmit through the bP to the underlying substrate. We conclude that oxide defects play the dominant role in the formation of a hysteresis in the transfer characteristics of bP FETs in this work and identify a hole capturing SiO_2 defect band at the bP conduction band edge as a likely candidate.

Thus, we have not only been able to identify the relevant defects, but also to deliberately adjust the location of defects within the bP FETs. This success enables controlled manipulation of the device's properties and thus represents a significant step forward in improving our understanding and control of hysteresis in bP FETs. Furthermore, the methodology employed in this work can be applied to various device architectures, such as capped 2D materials or 2D heterostructures, to fine-tune their respective memory and electrical properties by adjusting the fluence and kinetic energy of the ions.

2. Results and Discussion

2.1. Device Architecture

Figure 1a shows an optical microscopy image of one of our bP devices after fabrication. The flake is contacted by Cr/Au leads with a thickness of 10 and 100 nm respectively, in a two-terminal configuration, with a channel length of 5 µm. Because of the green-yellow color we can attribute a thickness of 20–30 layers (corresponding to a height of 10–20 nm) to the bP flake.[47] The inset shows an atomic force microscopy (AFM) linescan of the flake on the upper-right side of the contact that has the same color contrast as the flake acting as the transistors' channel. From the linescan, we extract a bP thickness of ≈13 nm (corresponding to 26 layers), which further supports the assessment of the thickness by the flakes' color. At this thickness, bP has already attained the bulk material bandgap of 0.3 eV.[7,8] Additionally, bP FETs fabricated with this channel thickness typically exhibit the highest mobility and $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio,[48] both crucial properties for non-volatile memory devices. Figure 1b displays a Raman spectrum measured in the region of the devices' channel. There are three modes that are generally observed for exfoliated bP, the A_{1g} mode at 362 cm^{-1}, the B_{2g} mode at 439 cm^{-1}, and the A_g^2 mode at 467 cm^{-1}.[49] The mode at 521 cm^{-1} stems from the underlying Si substrate. Figure 1c shows a schematic representation of our device characterization setup. The bP is placed onto a Si/SiO_2 substrate with an oxide thickness of 285 nm and is electrically contacted by the source and the drain contact. The voltage applied between these contacts, driving the current I_{DS}, is called V_{DS}. Additionally, the voltage V_{GS} is applied between the source contact and the silicon backgate to modulate the charge carrier density of the device.

2.2. Electrical Characterization Before Irradiation

Figure 1d shows a typical output characteristics for our devices, i.e., measuring the current between the two contacts (I_{DS}) due to the applied voltage (V_{DS}) with the backgate voltage (V_{GS}) as a control parameter. We measure a linear dependence of I_{DS} with V_{DS} and a change of the slope of the linear behavior when applying V_{GS}. This is indicative of ohmic contacts between the metal contacts and the bP channel. For negative V_{GS} the slope increases while it decreases for positive V_{GS}. This is the typical behavior of a p-type semiconductor. Overall, these are common observations for such devices.[18,25,48] Figure 1e shows the transfer characteristics of our device on a linear scale, where I_{DS} is measured for a constant V_{DS} while V_{GS} is swept from negative to positive values. The increase of I_{DS} with negative V_{GS} is again the typical behavior of a p-type semiconductor. From the transfer characteristics we can derive the field-effect hole mobility of our device by fitting

$$\mu_h = \frac{\partial I_{DS}}{\partial V_{GS}} \cdot \frac{1}{C_{ox} V_{DS}} \frac{L}{W} \tag{1}$$

to the linear region. $\frac{\partial I_{DS}}{\partial V_{GS}}$ is the slope of the transfer curve for $V_{GS} >> V_{DS}$, C_{ox} is the capacitance of the gate oxide, which is $1.21 \cdot 10^{-8}$ F cm^{-2} in our case, and L is the length and W the width of the devices' channel. From the optical image in Figure 1a we have estimated these to be $W = 6.8$ µm and $L = 5.1$ µm for the device used in this work. Thus, the calculated field-effect hole mobility for our device is $\mu_h = 100.2$ cm^2 V^{-1}s^{-1}, in accordance with the typical values in devices with similar bP thicknesses as reported in previous studies.[50–52] The inset in Figure 1e shows the transfer characteristics of the device on a logarithmic scale, when the gate voltage is not only swept from negative to positive values, but additionally back from negative to positive values again at a constant $V_{\mathrm{DS}} = 50$ mV. This measurement leads to the observation of a hysteresis in the transfer characteristics, which is in general explained by charge trapping and detrapping at impurities and defects within the device.

2.3. Influence of HCI Irradiation on Electrical Properties

We now start discussing the influence of HCI irradiation at a kinetic energy of 180 keV on the electrical properties of the bP FETs. The device was irradiated with increasing ion fluence starting from $1 \cdot 10^{10}$ ions cm^{-2} up to a total fluence of $1 \cdot 10^{12}$ ions cm^{-2} and electrically characterized after each irradiation step. First, we calculate the conductance of our devices for each irradiation step by linear fitting the output characteristics for $V_{\mathrm{GS}} = 0$ V and plot the result in **Figure 2a**. For the first irradiation step the overall conductance decreases slightly, but for the additional irradiation steps the conductance increases with increasing ion fluence. This increase in conductance with increasing defect density seems counter-intuitive at first but has also been observed for ion irradiation of other 2D FETs.[42,53]

In our case, the increase in conductance can be explained by the increase of p-doping due to the irradiation. In Figure 2b, we plot the threshold voltage of the device (V_{th}) for the different irradiation steps. The threshold voltage increases to higher positive

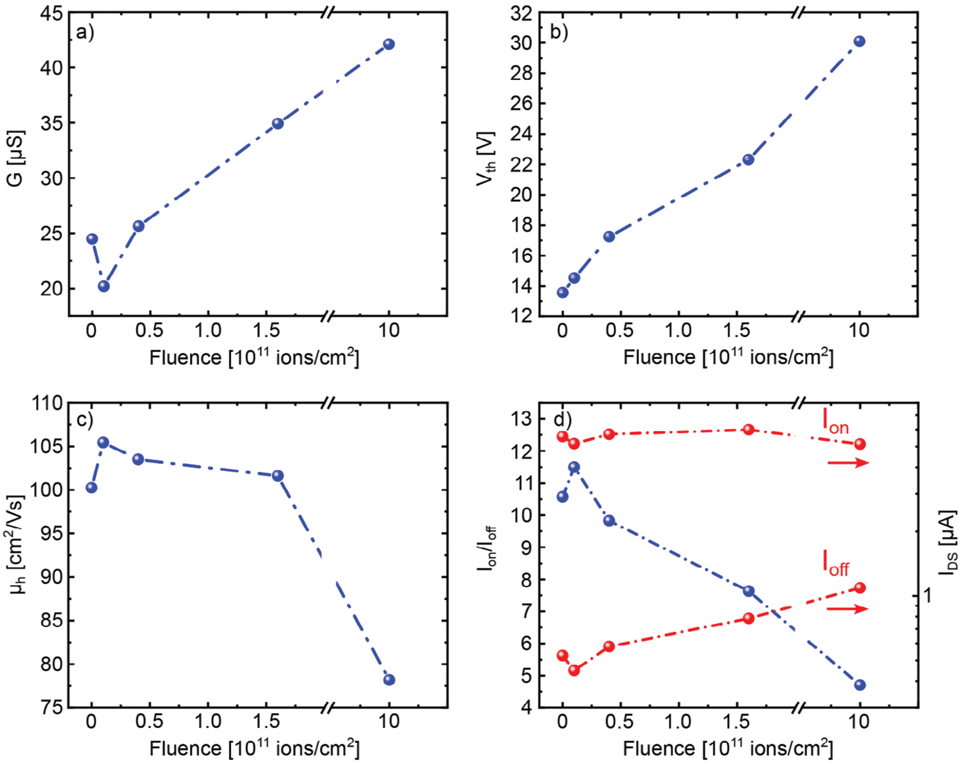

Figure 2. a) Conductance of the device obtained from the output characteristics after each irradiation step. b) Threshold voltage (V_{th}) of the device obtained from the transfer characteristics after each irradiation step. c) Effective hole field-effect mobility of the device after each irradiation step. d) I_{on}/I_{off} ratio (blue) and separately values for I_{on} and I_{off} respectively (red) extracted from the transfer characteristics of the device at V_{GS} = -50 V (on) and V_{GS} = 50 V (off) after each irradiation step.

values with increasing ion fluence. This is characteristic of additional p-doping induced due to the irradiation. For the highest irradiation fluence V_{th} increases by ≈16 V, which corresponds to an increase of the hole concentration of $\approx 1.2 \cdot 10^{12}$ cm^{-2} by calculating:

$$\Delta p = C_{ox} \frac{\Delta V_{th}}{q} \tag{2}$$

Here, q is the elementary charge. Single phosphorus vacancies have been experimentally observed to have a p-doping effect.[54] Additionally, more complex defects, like substitutional oxygen, oxygen bridge-type defects, and phosphorus self-interstitials are at least theoretically predicted to facilitate p-doping.[55,56] At the high kinetic energy used here, a large number of collisions will take place within the bP channel causing various kinds of defects. This is demonstrated in **Figure 3**, where a SRIM simulation of Xe^+ ions with a kinetic energy of 180 keV impinging onto a bP/SiO_2 heterostructure is shown. The thickness of the bP layer and the SiO_2 layer is 13 and 167 nm, respectively. These thicknesses are chosen to reflect the structure of the channel of the bP FET. Orange lines show the trajectories of phosphorus atoms of the bP channel, which are set in motion by a collision with an incoming Xe^+ ion and displace additional phosphorus atoms. These displacements correspond to the creation of defects in the bP channel, such as single vacancies and more complex defects. Light blue lines and pink lines show such paths for silicon and oxygen atoms of the SiO_2 substrate, respectively, demonstrating that at a kinetic energy of 180 keV a lot of defect creation is not only expected to take place in the bP channel but also in the underlying substrate. Charged defects in the underlying substrate can also influence the doping of such devices by an additional gating effect. For bP in particular it was demonstrated that a hole defect band in the SiO_2 substrate can lead to p-doping of the device under test by injecting additional holes into the channel if the Fermi level of the bP matches with the energetic position of the hole defect band.[33] Therefore, the increase in p-doping due to irradiation is to be expected if the irradiation leads to an increased density of oxide defects.

Next, we want to discuss the influence of the irradiation on the charge carrier mobility of our device. The hole mobility of the device for the different irradiation steps is shown in Figure 2c. Up to a fluence of $1.6 \cdot 10^{11}$ ions cm^{-2} there is no clear influence of the irradiation on the mobility. Only at the highest fluence a reduction of the mobility of ≈20% can be observed. The degradation of the mobility is caused by defects introduced into the channel of the device by the irradiation, that act as scattering centers for the charge transport. At lower fluences, the density of these defects is too small to have a noticeable effect on the mobility, especially since the channel material is ≈26 layers thick.

The I_{on}/I_{off} ratio is an important parameter that assesses the switching capabilities of a transistor. We determine the I_{on}/I_{off} ratio by taking I_{DS} at $V_{GS} = -50$ V and $V_{GS} = 50$ V into account and plot the result in Figure 2d, with the values for I_{on} and I_{off}

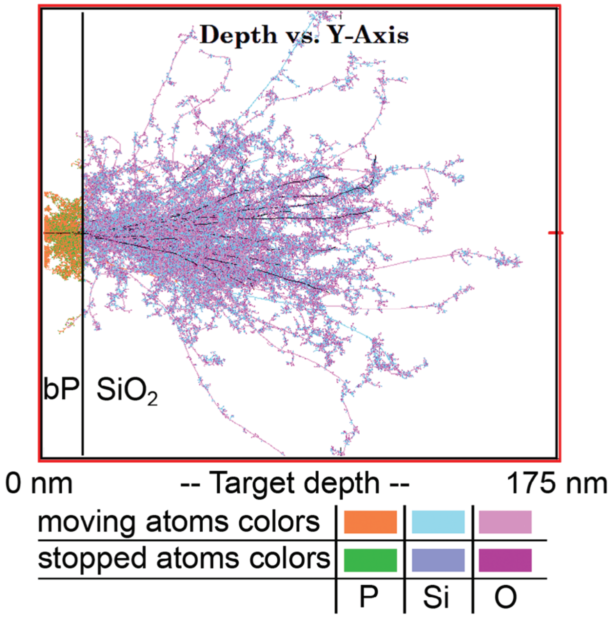

Figure 3. SRIM Simulation[57] for the irradiation of the heterostructure of bP/SiO_2 (thickness: 13/162 nm) with Xe^+ ions with a kinetic energy of 180 keV. Black lines show the mean trajectories of the Xe^+ ions in the irradiated system. Orange lines show the trajectories of phosphorus atoms of the bP channel, which are set in motion by a collision with an incoming Xe^+ ion and then displace additional phosphorus atoms. Light blue lines and pink lines mark such paths for silicon and oxygen atoms of the SiO_2 substrate respectively. Green dots mark the location, where the movement of the phosphorus atoms stops. This is shown by dark-blue and purple dots for silicon atoms and oxygen atoms of the SiO_2 substrate, respectively.

plotted in red respectively. The I_{on}/I_{off} ratio starts with a value of ≈10.5 and degrades for fluences higher than $1 \cdot 10^{10}$ ions cm^{-2}. The low I_{on}/I_{off} ratio is to be expected and can be attributed to the small bandgap of merely 0.3 eV, for thicknesses above ≈10 nm, as is the case for the flake used here. This decrease of the I_{on}/I_{off} ratio is mainly driven by the increase of I_{off}, while I_{on} is found to be quite stable. The increase of I_{off} is due to the right-shift of the transfer characteristics caused by the increase in p-doping with higher irradiation fluences. Note, that the small deviation from the general trend at the lowest fluence in Figure 2a,c,d might be due to the initial removal of chemisorbed species by electronic excitation due to the high charge state of the incoming ion.[58,59] All in all, these findings illustrate the strong resilience of bP FETs to ion irradiation, which is an essential characteristic for prospective applications in environments with high radiation levels, such as outer space or reactor environments.

2.4. Influence of HCI Irradiation on the Hysteresis and Memory Properties

Now we move on to discuss the influence of the HCI irradiation on the hysteresis and memory properties of the device. **Figure 4a** shows the hysteresis in the transfer characteristics of our device when sweeping V_{GS} from –50 to 50 V and back before and after the different irradiation fluences. We calculate the width of the hysteresis (H_w) at $I_{DS} = 2$ μA as it is marked by the orange line in Figure 4a and plot its value for the different irradiation fluences in Figure 4b. The hysteresis width increases strongly up to a fluence of $1.6 \cdot 10^{11}$ ions cm^{-2} and shows a saturation behavior for the highest fluence of $1.0 \cdot 10^{12}$ ions cm^{-2} leading to an increase of ≈70% compared to its initial value. As discussed above, the occurrence of a hysteresis in 2D FETs is generally explained by charge trapping and detrapping at defects and impurities. Thus, the increase of defects in the device caused by the ion irradiation leads to the widening of the hysteresis observed here. While some works propose that defects in the bP channel are causing the hysteresis,[14,25] other works point at oxide defects playing the dominant role for this phenomenon.[33] Due to the high kinetic energy of 180 keV used here, defects are not only created in the bP channel itself but also in the underlying substrate. Therefore both types of defects could potentially be responsible for the observed effect.

To test the performance of our device as a non-volatile memory device we applied ± 50 V gate pulses while sourcing a constant voltage $V_{DS} = 50$ mV and measured the transient behavior of the corresponding current I_{DS} at $V_{GS} = 0$ V. In Figure 4c, this measurement is shown for the device prior to the first irradiation. After a rapid increase/decrease of the current I_{DS} for the positive/negative gate pulse, it stabilizes at two distinct memory states, which remain separated for the observed time period of ≈10 min. By fitting a bi-exponential function

$$I_{DS} = I_{DS,0} + A_1 \cdot \exp - \left(\frac{x - x_0}{\tau_1} \right) + A_2 \cdot \exp - \left(\frac{x - x_0}{\tau_2} \right) \quad (3)$$

to the transient behavior of I_{DS} after the gate voltage has been turned off, we find two time constants $\tau_1 \approx 17$ s and $\tau_2 \approx 240$ s after the positive gate pulse. The time constants for both gate pulses (positive and negative) are roughly the same. These two time constants point at two different defect types being present in our device. The shorter time constant τ_1 can be attributed to fast trap states typically located in the bP channel and the bP/SiO_2 interface.[60,61] The second, much longer time constant τ_2 points to slow trap states that can either be located in the oxide or in the bP channel as deep defect states in the bandgap. These defects typically have very long trapping/detrapping times extending up to days.[25,62,63]

By calculating the difference between $I_{DS,0}$ after the positive and after the negative gate pulse, respectively ($I_{DS,0}$ (+) - $I_{DS,0}$ (−)), we evaluate the so-called memory window, i.e., the separation of the two memory states of our device after the irradiation steps and plot the result in Figure 4d. It can be seen that the memory window increases by ≈30% up to a fluence of $1.6 \cdot 10^{11}$ ions cm^{-2} and then slightly decreases for the highest fluence of $1 \cdot 10^{12}$ ions cm^{-2}. Nevertheless, it still remains wider than prior to any irradiation. A wide memory window is an important property for memory devices, to prevent unwanted switching and therefore guarantee stable device operation. Note, that for the type of device used here, long retention times up to 30 min and a stable endurance for more than 200 cycles have already been reported in our previous works.[25,27,52] The increase of the memory window is consistent with the increase of the hysteresis width with increasing ion fluence. As the irradiation increases the density of trapping/detrapping defects, the hysteresis width and height increase too. For the highest fluence a second effect influences the

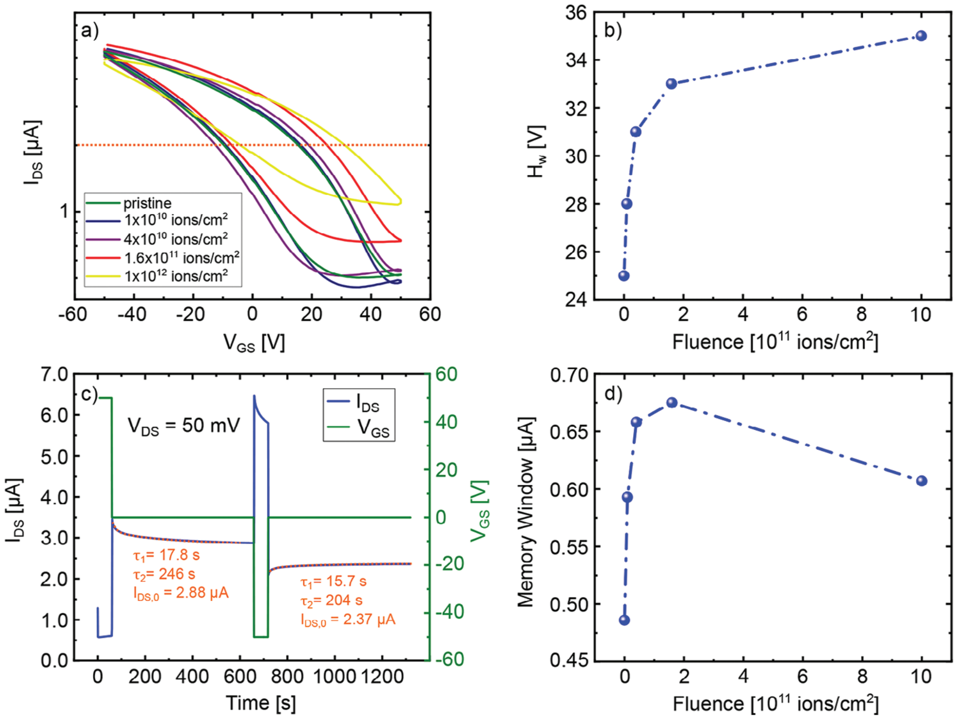

Figure 4. a) Transfer characteristics of our device for a forward–backward sweep after the different irradiation steps. b) Hysteresis width extracted from a) for the different irradiation steps. c) Transient behavior of our device prior to any ion irradiation for one set-read-reset-read cycle. d) Memory window size ($I_{DS,0}(+)$ - $I_{DS,0}(-)$) extracted from the transient behavior of our device after each irradiation step.

memory window: Because of the additional p-doping effect of the irradiation, there is a shift of the transfer characteristics (and by that of the hysteresis) to higher positive gate voltages, so that the memory window is evaluated rather in the saturation range of the hysteresis compared to the other measurements. In this part of the hysteresis, its height is typically observed to be much smaller, explaining the slight decrease of the memory window after the highest irradiation fluence measured here.

2.5. Determining the Location of the Defect Responsible for the Hysteresis

To better understand the results presented above and the procedure described in this work we want to discuss the nature of the defects responsible for the manipulation of the electrical and hysteretic properties in more detail.

We start by pinpointing the location of the defects in our device, whether they are located in the bP channel or in the underlying substrate. For that, we investigated another device, with a bP thickness of 55 nm (see AFM linescan in **Figure 5a**). We performed the same characterizations as before, but the irradiations were carried out with Xe^{30+} ions with a kinetic energy of only 20 keV. At that kinetic energy the defect creation in this device will take place exclusively in the bP channel because the ions cannot reach the underlying oxide, as predicted by the SRIM calculations in Figure 5a. Figure 5b–d shows the electrical characterization of the device for the different irradiation steps by displaying the conductance, hole mobility, and threshold voltage, respectively. From this data we find that these electrical properties display the same qualitative behavior as it was shown in Figure 2 for the device irradiated with ions with the kinetic energy of 180 keV. For **Figure 6a** we extract the size of the memory window and the width of the hysteresis (H_w) for the non-irradiated device and after the irradiations with the lower kinetic energy. The device's memory properties are clearly unaffected by ion irradiation at a kinetic energy of 20 keV. This is evident as both the memory window and hysteresis width remain constant up to a fluence of $1.6 \cdot 10^{11}$ ions cm^{-2}, the fluence at which the most significant effect of irradiation was noted for the irradiation with a kinetic energy of 180 keV. This leads us to the conclusion that the alteration of electrical properties stems from defects within the bP channel, such as vacancies and lattice distortions. However, the defects accountable for the heightened hysteresis and better memory properties of our bP FETs post-irradiation, are situated either at the bP/SiO_2 interface or within the oxide layer.

To further confirm this claim, we investigated the subthreshold swing (SS) of the devices for the irradiations with a kinetic energy of 180 and 20 keV, respectively. The subthreshold swing is defined as the change needed in gate voltage to increase the drain-source current of the transistor by one decade:

$$SS = \frac{dV_{GS}}{d\log(I_{DS})} \approx \log(10)\frac{kT}{q}\left(1 + \frac{C_{it} + C_{dl}}{C_{ox}}\right) \tag{4}$$

with q the electric charge, k the Boltzmann constant, $T = 300$ K and C_{it}, C_{dl}, and C_{ox} as the capacitance of the interface trap states, the depletion layer and the oxide, respectively. Because of the very

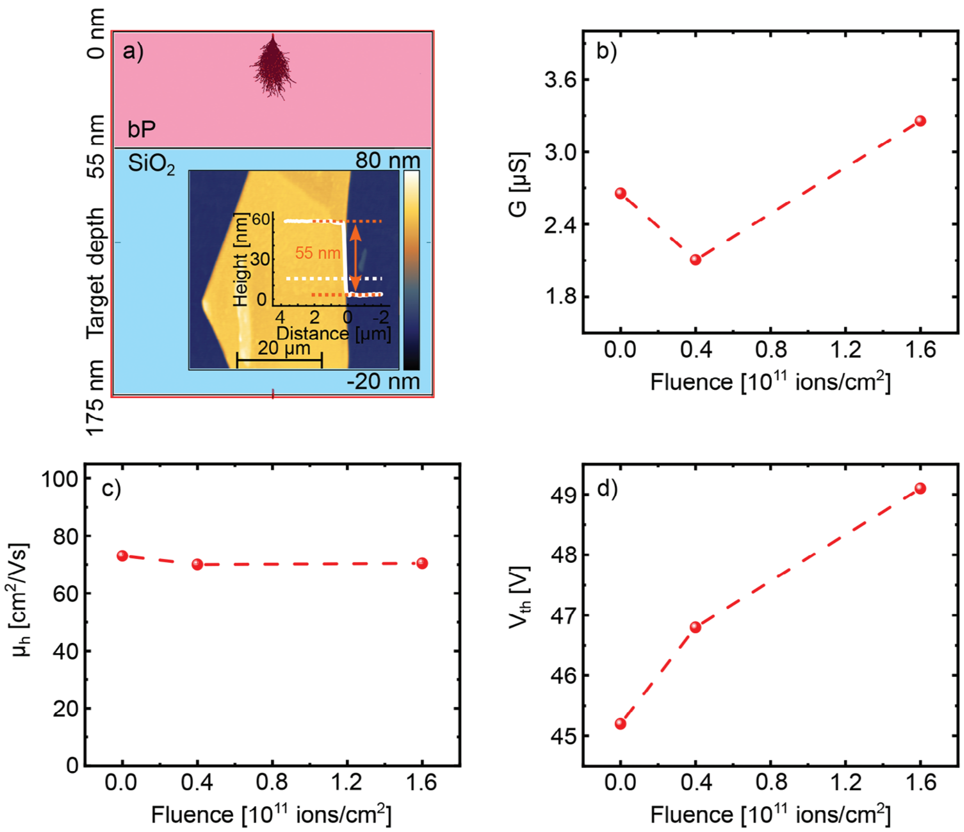

Figure 5. a) SRIM simulation[57] of the irradiation of a bP FET with a channel thickness of $\approx$ 55 nm with Xe^+ ions with a kinetic energy of 20 keV. The simulation shows the paths of the incoming Xe^+ ions, demonstrating that no ions reach the SiO_2 substrate. The inset shows an AFM image of the bP FET that was irradiated with Xe^{30+} ions at a kinetic energy of 20 keV with a linescan that demonstrates that the thickness of the bP is $\approx$ 55 nm. The position of the linescan is marked by the white dotted line. b)-d) Conductance, hole mobility, and threshold voltage of the device shown in the AFM image in a) for the different irradiation steps with Xe^{30+} ions at a kinetic energy of 20 keV.

high SS of 43 V dec^{-1} before the irradiation we assume C_{dl} to be negligible compared to C_{it}. With

$$D_{\mathrm{it}} = C_{\mathrm{it}}/q^2 \tag{5}$$

it follows directly, that SS increases with increasing interface trap density D_{it}.

In Figure 6b we plot the normalized SS for the irradiations for both kinetic energies. For the lower fluence of $4.0 \cdot 10^{10}$ ions cm^{-2} the effect of the irradiation is within the measurement resolution. However, there is a strong increase for a fluence of $1.6 \cdot 10^{11}$ ions cm^{-2} after the irradiation with E_{kin} = 180 keV but not for the irradiation with E_{kin} = 20 keV, as only the ions with the higher kinetic energy reach the underlying oxide and are indeed creating defects there. From our data we calculate an increase in interface trap density of $\Delta D_{\mathrm{it}} = 1.29 \cdot 10^{12}$ cm^{-2}eV^{-1} due to the irradiation.

Therefore, we propose the following explanation for the results in our work and the effect of the irradiation on our devices: The left side of Figure 6c represents a schematic band-diagram of the bP/SiO_2 interface in our devices prior to irradiation. Note, that the energetic positions of the defects in the bP bandgap are arbitrarily selected. Defect levels represented by black lines signify defects with time constants for trapping/detrapping events that are sufficiently slow to influence the transfer characteristics during a gate voltage sweep. Conversely, green lines indicate defects characterized by time constants too fast to contribute to the hysteresis. These defects undergo trapping/detrapping events within, e.g., the forward gate voltage sweep and thus do not affect the current in the channel during the backward gate voltage sweep.

The defect states located in the SiO_2 at the bPs conduction band edge have been previously addressed concerning their role in the hysteresis of bP FETs.[33] Following our observation of two time constants in the transient behavior in Figure 4c, there must be a second type of defect responsible for the hysteresis being present. As discussed earlier, we attribute the shorter time constant to defects in the bP channel (depicted as black lines within the bP bandgap). The green lines represent defects also present in bP, not influencing the hysteresis, but potentially impacting other electrical properties in our devices.

We conclude, that irradiation with a high enough kinetic energy for the ions to reach the underlying substrate, increases the density of the defects located in the SiO_2 at the bPs conduction band edge as well as the density of defects in the bP. The latter have short enough time constants (green lines) to not contribute to the hysteresis, but they do play a role in altering electrical properties such as doping and mobility (see Figure 6c). However, the density of defects in the bP that can indeed contribute to the

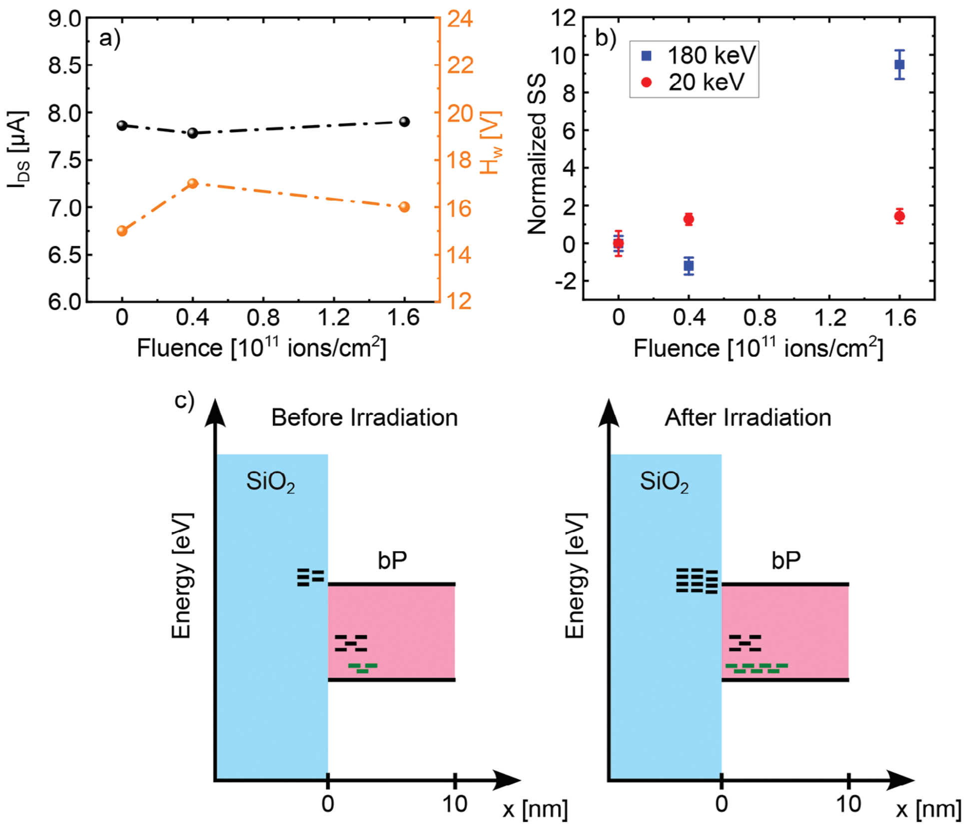

Figure 6. a) Size of the memory window (ΔI_{DS}) and width of the hysteresis (H_w) of the bP FET irradiated with Xe^{30+} ions at a kinetic energy of 20 keV for different irradiation fluences. b) Comparison of the normalized subthreshold swing of the bP FETs irradiated with Xe^{30+} ions at a kinetic energy of 20 keV and 180 keV for different irradiation fluences. c) Schematic of the banddiagramm of the SiO_2/bP system present in our devices. Black lines indicate defects with trapping/detrapping times of charge carriers that are sufficiently slow so that they can influence the transfer characteristics of the bP FETs during a gate voltage sweep, thereby contributing to the hysteresis. Green lines indicate defects with trapping/detrapping times of charge carriers that are too fast to influence the transfer characteristics of the bP FETs during a gate voltage sweep.

hysteresis is not increased by the irradiation. Possible candidates for these kind of defects are, e.g., impurities already present in the bulk material or more complex defects that cannot be created by the ion irradiation. With irradiation at a kinetic energy of only 20 keV, no defect creation occurs in the substrate. Instead, only the density of defects within bP, characterized by time constants too short to contribute to the hysteresis (illustrated by green lines), increases. Therefore, the irradiation at a kinetic energy of 20 keV influences the electrical properties without affecting the hysteresis.

3. Conclusion

We have studied the electrical and memory properties of bP FETs on Si/SiO_2 substrates before and after irradiation with Xe^{30+} ions at a kinetic energy of 180 and 20 keV, respectively. For both kinetic energies we found an increase in conductance and p-doping of our device due to the irradiation. The hole mobility drops to only ≈20% at the highest fluence of $1.0 \cdot 10^{12}$ ions cm^{-2} at a kinetic energy of 180 keV, demonstrating that the electrical properties of such devices can be well-controlled by highly charged ion irradiation. We measure a hysteresis in the transfer characteristics of our device prior to irradiation and utilize it to realize a non-volatile memory device with this simple device architecture, where the SiO_2 substrate acts as both, charge-trapping and charge-blocking layer. By irradiation at a kinetic energy of 180 keV we obtain a strong increase of the width of the hysteresis and the memory window. We find an optimal fluence of $1.6 \cdot 10^{11}$ ions cm^{-2}, at which the largest memory window is measured, while there is still no observable degradation of the mobility. We could unambiguously attribute this remarkable behavior to additional, irradiation-induced defects in the underlying substrate, rather than within the bP itself. This is evidenced by our demonstration, that the irradiation with Xe^{30+} ions at a low kinetic energy of 20 keV, which prevents the ions from penetrating through the bP into the underlying SiO_2, does not result in improved memory properties.

4. Experimental Section

Device Fabrication: bP bulk material (purchased from smart elements) was used to exfoliate bP flakes on a highly doped p-type Si substrate (resistivity 0.001–0.005 Ωcm) covered by 285 nm dry-grown SiO_2. To fabricate the devices, freshly exfoliated samples were examined using optical microscopy to identify appropriate flakes for subsequent photolithography processing. Following the standard photolithography procedure using the maskless optical lithography machine "SMART PRINT UV" from microlight3D, 10 nm of Cr and 100 nm of Au were deposited through electron-beam (Cr) and thermal evaporation (Au) at a process pressure of $1 \cdot 10^{-5}$ mbar to establish electrical contacts with the bP flakes.

Electrical Characterization: Electrical characterization of the devices was performed with a Linkam Stage THMS350EV connected to a Keithley 2612B source-measure-unit. All electrical measurements in this work were performed under a vacuum of $1 \cdot 10^{-2}$ mbar.

Raman and Atomic Force Microscopy: The Raman spectra were collected with a WITec alpha300 RA confocal Raman spectrometer. Atomic force microscopy (AFM) measurements were performed by the WITec alpha300 RA tapping mode AFM utilizing "NanoSensors" PPP NCHR extra sharp, reflective coated tips. The topography was measured with a tip velocity of 1 line s^{-1} with an image resolution of 512 lines/image × 512 points/line. The AFM results were analyzed and visualized by "Gwyddion 2.6".

Ion irradiation: To irradiate the devices, the HICS beamline was utilized.[44,64] In this set-up highly charged xenon ions were generated using a commercially available electron beam ion source (EBIS) from Dreebit GmbH, Germany.[65] A kinetic energy of 180 keV (1.4 keV amu^{-1}) and 20 keV (0.16 keV amu^{-1}), along with an ion charge state of 30+ and a potential energy of 15.4 keV (0.1 keV amu^{-1}), were selected using a sector magnet. Ion irradiation was conducted under ultra-high vacuum conditions (pressure $\approx 4 \cdot 10^{-9}$ mbar), with each sample exposed to a total fluence ranging from ($1.0 \cdot 10^{10} - 1.0 \cdot 10^{12}$) ions cm^{-2}. Throughout the irradiation process, the entire device, including its electrical contacts, was hit by ions due to the spatial extent ($\approx$1 mm^2) of the ion beam.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D materials, black phosphorus, defects, field-effect transistor, ion irradiation, non-volatile memory device

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